AMENDMENT TO THE CLAIMS

Please cancel claims 21 and 29;

Please amend claims 16, 22 and 25; and

Please add new claims 30-39 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-15 (Canceled).

16. (Currently Amended) A method for reducing diffusion of an N type impurity in a SiGe-based substrate, the method comprising steps of:

forming source and drain extension regions in an upper surface of the SiGe-based substrate; and

ion implanting an interstitial element into the source and drain extension regions to reduce vacancy concentration in the source and drain extension regions and to form low-vacancy regions that substantially overlap the source and drain extension regions.

17. (Previously Presented) The method of claim 16, wherein the interstitial element is Si or O.

18. (Original) The method of claim 16, further comprising a step of forming source and drain regions.

Claims 19-21 (Canceled).

22. (Currently Amended) The method of claim ~~21~~ 16, wherein the step of ion-implanting the interstitial element comprises a step of ion-implanting the interstitial element at an implantation concentration of approximately 1×10^{14} atoms/cm^2 to 1×10^{16} atoms/cm^2 and at an implantation energy of approximately 0.3 KeV to 100 KeV.

23. (Previously Presented) The method of claim 22, wherein a concentration peak of the interstitial element and a concentration peak of the N type impurity in the source and drain extension regions are formed at substantially the same depth from an upper surface of an Si cap layer.

24. (Previously Presented) The method of claim 23, wherein the concentration peak of the interstitial element is formed at a depth of approximately 10 Å to 20000 Å from the upper surface of the Si cap layer.

25. (Currently Amended) The method of claim ~~21~~ 16, further comprising a step of annealing.

26. (Previously Presented) The method of claim 25, wherein the step of annealing is performed at a temperature of approximately 700° C to 1200° C for approximately 1 second to 3 minutes.

27. (Previously Presented) The method of claim 17, further comprising a step of forming source and drain regions in the upper surface of the SiGe-based substrate, the source and drain regions containing the N type impurity and overlapping the source and drain extension regions.

28. (Previously Presented) The method of claim 27, further comprising a step of providing an interstitial element in the source and drain regions.

Claim 29. (Canceled).

30. (New) The method of claim 16, further comprising forming an Si cap layer on the SiGe based substrate and straining biaxially in tension the Si cap layer to match an underlying relaxed SiGe lattice.

31. (New) The method of claim 16, further comprising forming sidewalls on side surfaces of a gate electrode before the ion implanting, whereby the gate electrode is protected from the ion implanting.

32. (New) The method of claim 16, wherein the vacancy concentration is reduced by annihilation of excess vacancies in the source and drain extension regions.

33. (New) The method of claim 16, wherein the ion implanting occurs before the forming.

34. (New) The method of claim 16, further comprising, before the ion implanting, forming sidewalls on side surfaces of a gate electrode, wherein the interstitial element comprises an N-type impurity.

35. (New) The method of claim 16, wherein the interstitial element creates additional interstitials which react with and annihilate excessive vacancies in the SiGe based substrate.

36. (New) The method of claim 16, wherein the ion implanting reduces an N-type impurity in source and drain regions, thereby improving roll-off characteristics.

37. (New) The method of claim 16, wherein the ion implanting is performed in a self-aligned manner by using a gate electrode as a mask.

38. (New) A method for reducing diffusion of an N type impurity in a SiGe substrate, the method comprising steps of:

forming an Si cap layer on the SiGe substrate;

forming a gate electrode on the Si cap layer;

forming sidewalls on sides of the gate electrode;

forming source and drain extension regions in an upper surface of the SiGe-based substrate; and

ion implanting an interstitial element into the source and drain extension regions to reduce vacancy concentration in the source and drain extension regions,

wherein the ion implanting occurs after the sidewalls are formed.

39. (New) A method for reducing diffusion of an N type impurity in a SiGe substrate, the method comprising steps of:

forming an Si cap layer on the SiGe substrate;

forming a gate electrode on the Si cap layer;

forming sidewalls on sides of the gate electrode;

forming source and drain extension regions in an upper surface of the SiGe substrate; and

reducing a vacancy concentration in the source and drain extension regions using ion implantation in order to annihilate excess vacancies or trap vacancies,

wherein the reducing occurs after the sidewalls are formed and forms low-vacancy regions that substantially overlap the source and drain extension regions.